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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/931,072 | 08/15/2001 | Erik Cota-Robles | 42390P10807 | 2890 |

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| EXAMINER | |
|---|---|
| BULLOCK JR, LEWIS ALEXANDER | |
| **ART UNIT** | **PAPER NUMBER** |
| 2195 | |

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/931,072 | COTA-ROBLES ET AL. | |
| | Examiner | Art Unit | |
| | Lewis A. Bullock, Jr. | 2195 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *2/16/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-8, 11-20, 23-29 and 31-34 are rejected under 35 U.S.C. 102(e) as being anticipated by NELSON (U.S. Patent 6,961,941 cited in action mailed May 20, 2005).

As to claim 1, NELSON teaches a method comprising: trapping, by a processor, a change in execution (via a world switch) among schedulable entities (worlds / schedulable entities) running on a virtual machine; and tracking an execution of a schedulable entity that is being switched in for execution as a result of the change in execution (via determining if another world switch is to occur / managing the resources of the world) (col. 10, lines 5-63; col. 16, lines 19-57; see also col. 8, lines 24-28).

As to claim 2, NELSON teaches the tracking is performed by a privilege entity (kernel) and further comprising: calculating, by the privileged entity (kernel), an estimated resource requirement (resource) for the schedulable entity (world) that is being switched in for execution from the tracking of a previous execution of the

schedulable entity (resources used by the previous world) (via proportional-share processor scheduling / or guaranteed minimum rates); and scheduling, by the privileged entity (kernel), the schedulable entity (world) that is being switched in for execution according to its estimated resource requirement (col. 16, lines 20-56).

As to claim 3, NELSON teaches the schedulable entities (worlds / separately scheduled entities) are selected from the group consisting of processes, threads, operating systems, and child virtual machine monitors (col. 10, lines 5-31). NELSON does not explicitly teach that the privileged entity is a virtual machine monitor. NELSON does teach that the kernel functions similar to a virtual machine monitor in that it handles the resources for the virtual machine (col. 16, lines 19-57) and therefore the kernel is inherently considered a virtual machine monitor.

As to claim 4, NELSON teaches the privileged entity (kernel) comprises: an idle detector to receive notice from the processor of the change in execution (world switch) and to derive a measured value for a schedulable entity that is being switched out of execution (guaranteed minimum rates); a proportional integral derivative (PID) controller logically coupled to the idle detector to receive the measured value and to calculate the estimated resource requirement required by the schedulable entity that is being switched out of execution (via using the rate or percentage of resources for the world in order to allocate resources); and a scheduler logically coupled to the PID controller to receive the estimated resource requirement and to determine a schedule of execution

for the schedulable entity that is being switched out of execution (via performing proportional-share processor resource scheduling) (col. 16, lines 20-56).

As to claim 5, NELSON teaches calculating an estimated resource requirement comprises: assigning an initial value as the estimated resource requirement for the schedulable entity that is being switched in for execution; reducing the estimated resource requirement for the schedulable entity if the schedulable entity completes execution before the estimated resource requirement is exhausted; and increasing the estimated resource requirement for the schedulable entity if the schedulable entity does not complete execution before the estimated resource requirement is exhausted (via performing proportional-share processor resource scheduling wherein an administrator can control the relative CPU rates by specifying the number of shares allocated to each world and can increase the number of shares) (col. 16, lines 20-56).

As to claim 6, NELSON teaches initiating by the privileged entity (kernel), the change in execution (a world switch via preemption or the world that is executing on the processor yields execution) (col. 10, lines 56-63).

As to claim 7, NELSON teaches the tracking of the execution is performed as part of the change in execution initiated by the privilege entity (via performing a world switch) (col. 10, lines 56-63).

As to claim 8, NELSON teaches initiating, by the processor, the change if the change in execution is being requested by the privileged entity (a world switch via preemption or the world that is executing on the processor yields execution) (col. 10, lines 56-63).

As to claim 11, NELSON teaches trapping a change in execution comprises: detecting an instruction to change between privilege and non-privilege modes (via being capable of performing a world switch wherein a the worlds are both privilege and non-privilege entities, i.e. higher and lower level entities) (col. 10, lines 10-63).

As to claim 12, NELSON teaches the schedulable entities are selected from the group consisting of operating system processes, operating system thread, and instruction streams to be executed by the processor (col. 10, lines 10-63).

As to claims 13-20, 23 and 24, reference is made to a machine readable medium that corresponds to the method of claims 1-8, 11 and 12 and is therefore met by the rejection of claims 1-8, 11 and 12 above.

As to claims 25-29 and 31-34, reference is made to an apparatus that corresponds to the method of claims 1-8, 11 and 12 and is therefore met by the rejection of claims 1-8, 11 and 12 above.

3. Claims 1, 9, 10, 13, 21, 22, 25, 30, 35 and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by LIM (U.S. Patent 6,795,966).

As to claim 1, LIM teaches a method comprising: trapping, by a processor, a change in execution among schedulable entities (state change of virtual processor instructions; via the processor executing virtual machine instructions which include an end instruction that changes the processor state) running on a virtual machine (col. 10, lines 8-45); and tracking an execution of a schedulable entity that is being switched in for execution as a result of the change in execution (via the virtual machine monitor saving and restoring the state of an executing virtual processor instruction) (col. 6, lines 30-65; col. 18, lines 1-20; see also col. 16, lines 34-44; co. 19, lines 36-58; col. 20, lines 38-67).

As to claim 9, LIM teaches trapping a change in execution comprises: detecting an instruction to change a state register that identifies a schedulable entity (via an end instruction or state instruction, i.e. a checkpoint request instruction / restore request instruction to switch state contexts) (col. 10, lines 8-45; col. 6, lines 30-65; col. 18, lines 1-20).

As to claim 10, LIM teaches comparing, by the processor, the state register that identifies a schedulable entity being switched in for execution with a state register that identifies a schedulable entity that is to be tracked, wherein the schedulable entity being switched into execution is tracked by the processor if the state register and the state

match register match (via using the checkpoint request instruction or restore request instruction to checkpoint or restore the state of the processors in to the various registers) (col. 6, lines 30-65).

As to claims 13, 21 and 22, reference is made to a machine readable medium that corresponds to the method of claims 1, 9 and 10 and is therefore met by the rejection of claims 1, 9 and 10 above.

As to claims 25 and 30, reference is made to an apparatus that corresponds to the method of claims 1 and 9 and is therefore met by the rejection of claims 1 and 9 above.

As to claim 35, refer to claim 10 for rejection.

As to claim 36, LIM teaches the schedulable entities are selected from the group consisting of operating system processes, operating system thread, and instruction streams to be executed by the processor (virtual processor instructions) (col. 6, lines 30-65).

### *Response to Arguments*

4. Applicant's arguments filed February 16, 2006 have been fully considered but they are not persuasive. Applicant argues that Nelson does not teach trapping, by a

processor, a world switch. The examiner disagrees. Nelson states whenever a processor encounters an error (such as an attempt to address memory outside of some permissible range, or a violation of some privilege requirement), or completes some requested tasks, it typically generates a fault or interrupt signal that the operating system senses and handles in any predetermined manner (col. 8, lines 24-28). In addition, a kernel which performs a world switch as detailed in col. 10, lines 5-63) executes on a processor. Therefore, Nelson teaches both explicitly at col. 8, lines 24-28 and inherently by the kernel which performs the world switch executing on a processor of a processor trapping a change in execution, via the kernel receiving an request for a change in execution or in interrupt signal indicating that a task is complete, i.e. a schedulable entity is complete and thereby switching to a new schedulable entity. Therefore, the rejection is maintained.

5. Applicant argues that Lim does not teach trapping, by a processor a change in execution among schedulable entities. The examiner disagrees. At column 16, lines 7-31, Lim teaches in order for the VMM to virtualize the existing system, the VMM sets the value of the hardware processor's global descriptor table register to point to the VMMs global descriptor table. This enables the virtual machine monitor to convert the system to execute either in binary translation mode, via the binary translation execution engine or in direct execution mode via the direct execution engine (col. 16, lines 34-44; co. 19, lines 36-58; col. 20, lines 38-67). Therefore, Lim teaches the claim language of trapping by a processor, a change in execution by setting, i.e. trapping a change in execution engines/modes. Therefore, the rejection is maintained.

***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (571) 272-3759. The examiner can normally be reached on Monday-Friday, 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 9, 2006

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER